Intel Core i7 Nehalem

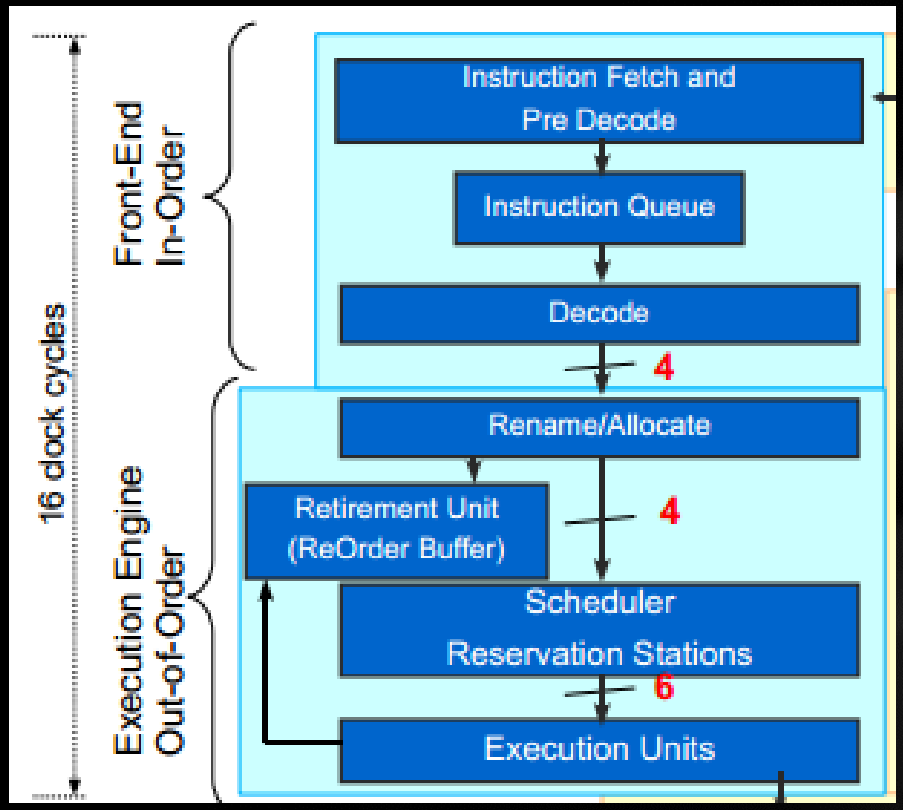
Derek Anderson, Matt Burrough, Gregory Robinson, Caleb Tote

Instruction Execution

Caleb Tote

Nehalem Core Pipeline

High-level view



- Front-End Pipeline (FEP)
  - In-order
  - Four decoders
- Execution Engine (EE)
  - Out-of-order
  - Dynamic scheduler
- Retirement Unit (RU)
  - In-order

Front-end Pipeline

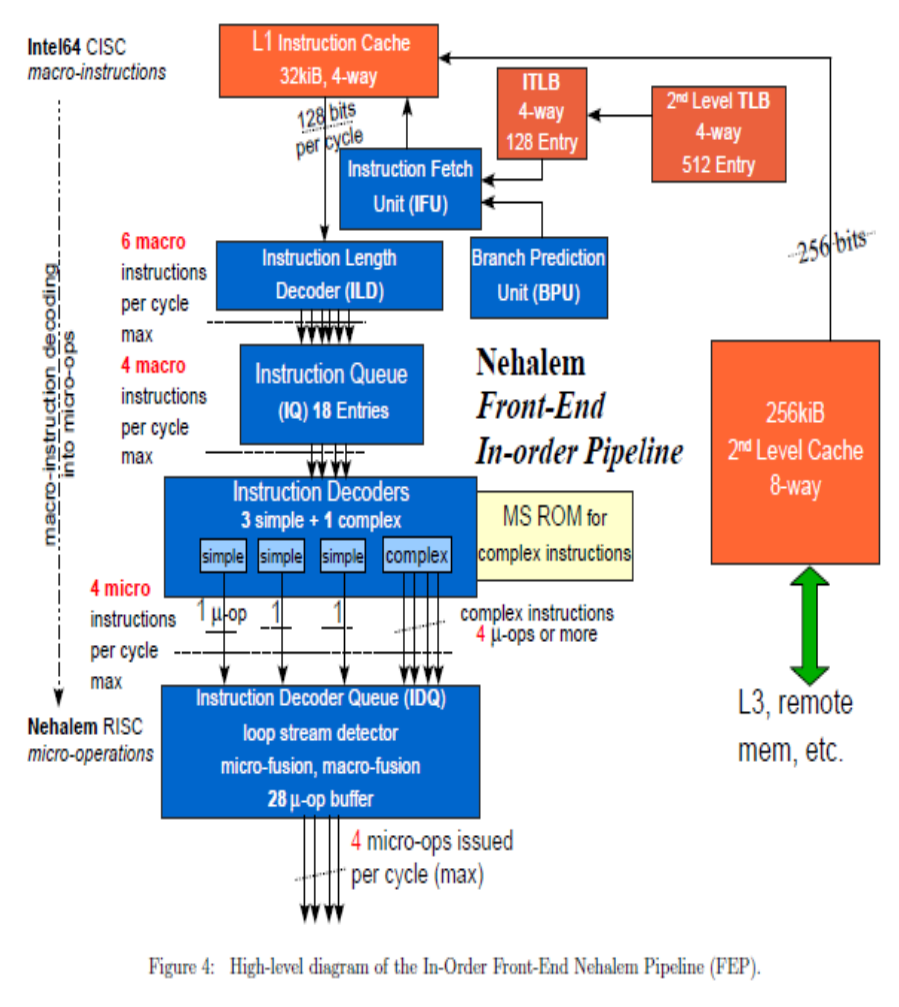
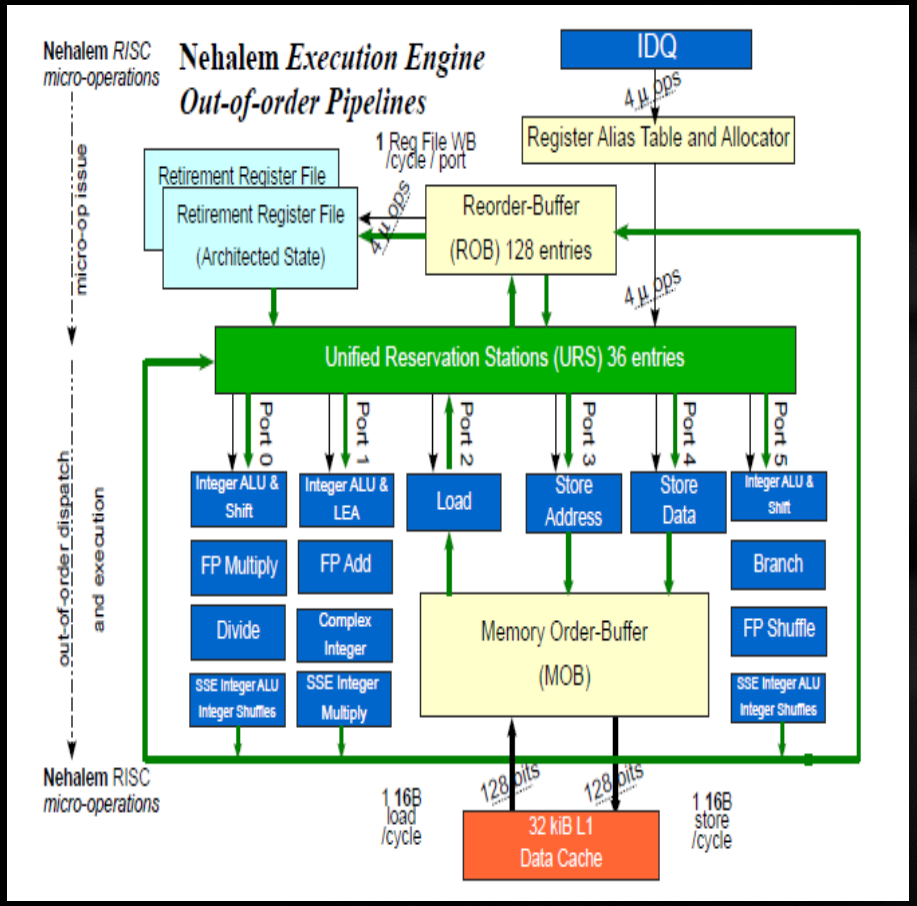


Figure 4: High-level diagram of the In-Order Front-End Nehalem Pipeline (FEP).

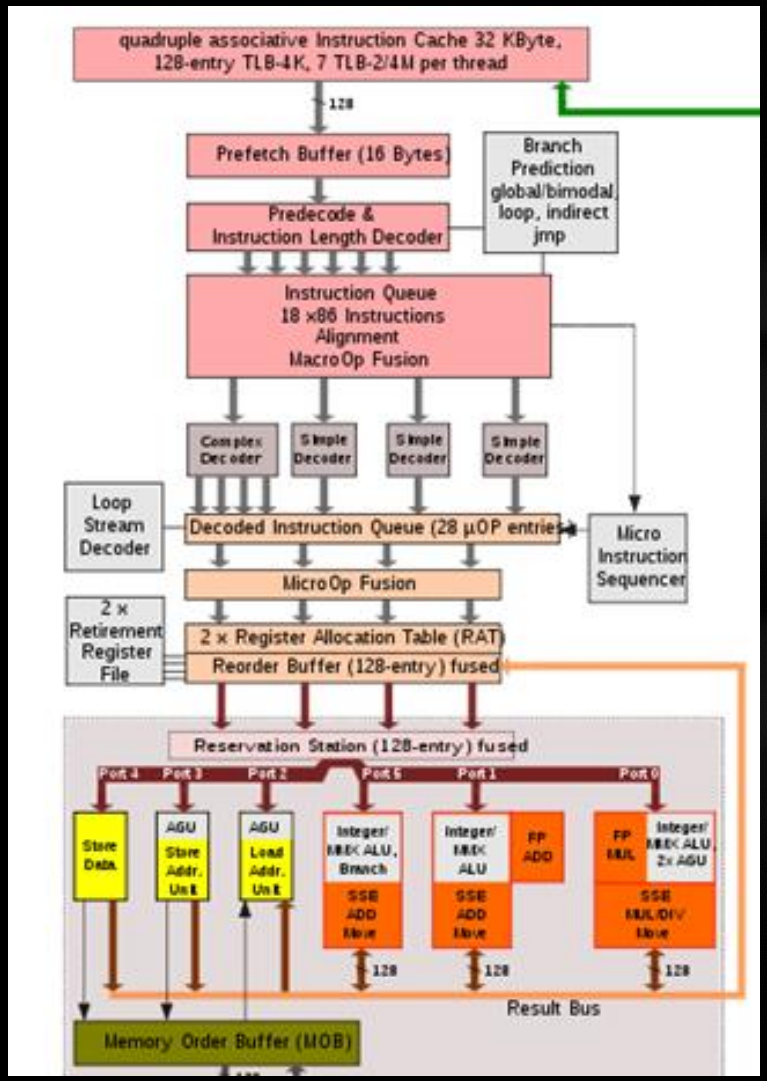
- Instruction Fetch Unit (IFU)
  - Instruction Pre-fetcher
  - Pre-decode logic of the IQ
- Branch-Prediction Unit (BPU)
  - Direct/Indirect calls & jumps
  - Conditional branches
- Branch Target Buffer (BTB)
- Micro-Fusion
- Macro-Fusion

Execution Engine



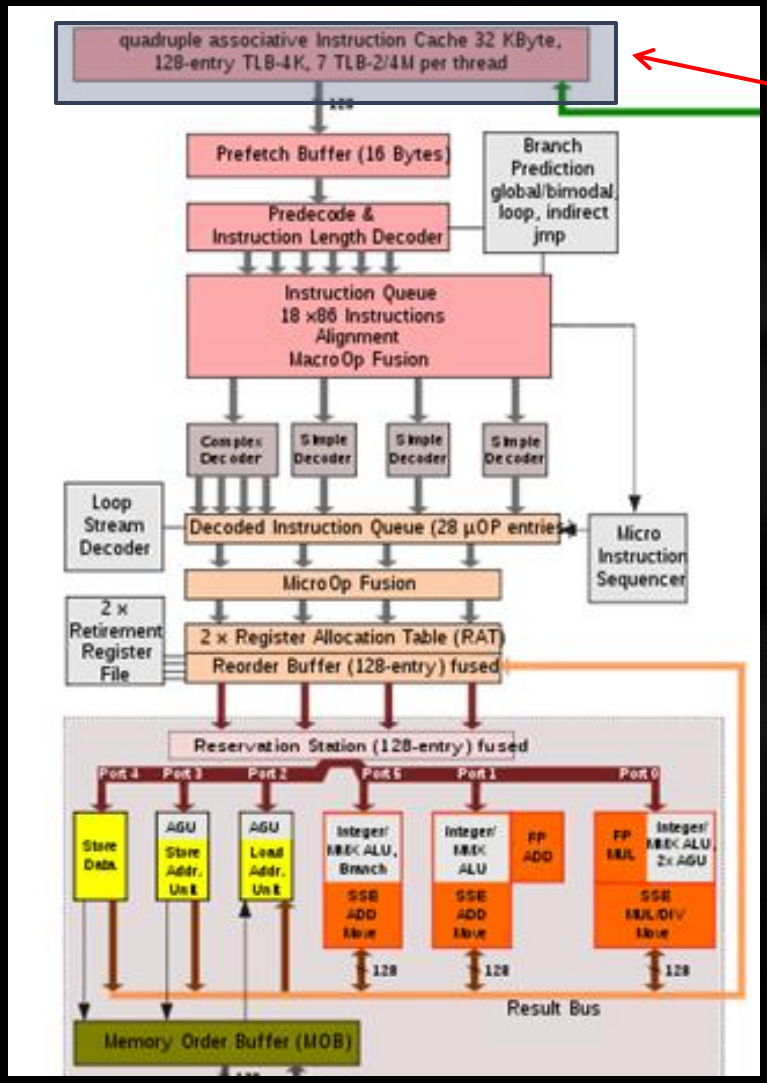
- Register rename and Allocation Unit
- Reorder Buffer
  - Micro-op tracking
- Unified Reservation Station
  - Que up to 36 Micro-ops
  - Schedule / Dispatch Micro-ops
- Memory Order Buffer
  - Speculative & out of order loads / stores

High-level Instruction Flow



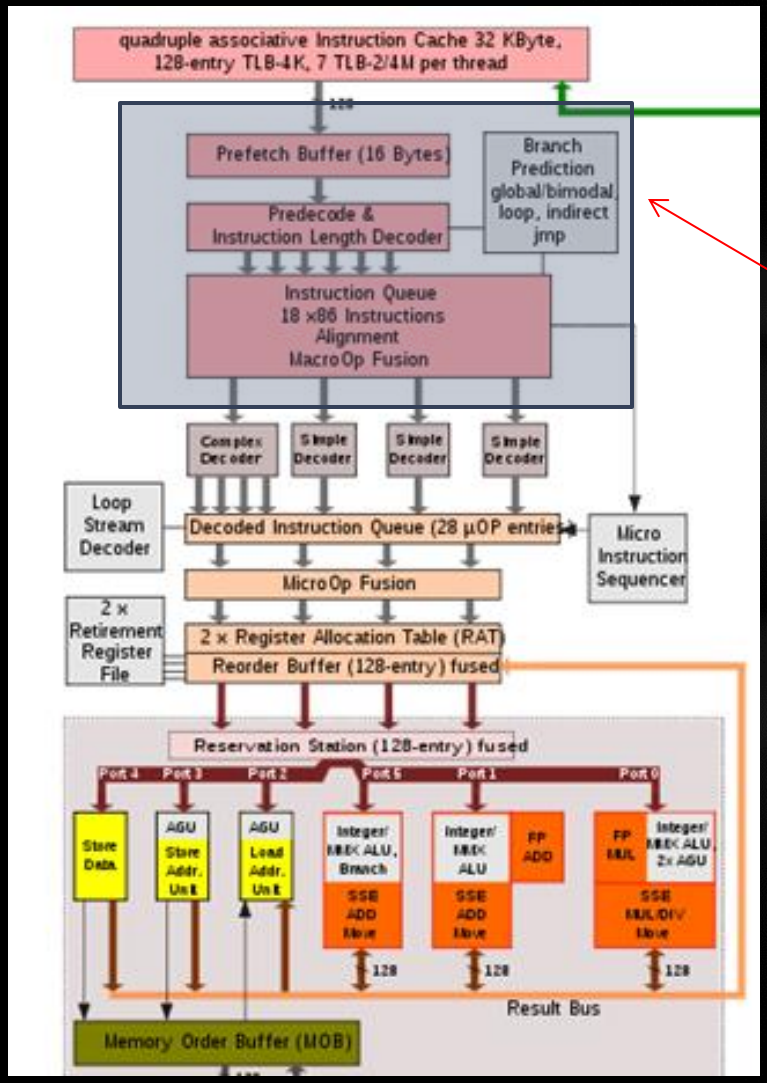
- Fetch
- Decode
- Optimize
- Execute
- Write

High-level Instruction Flow



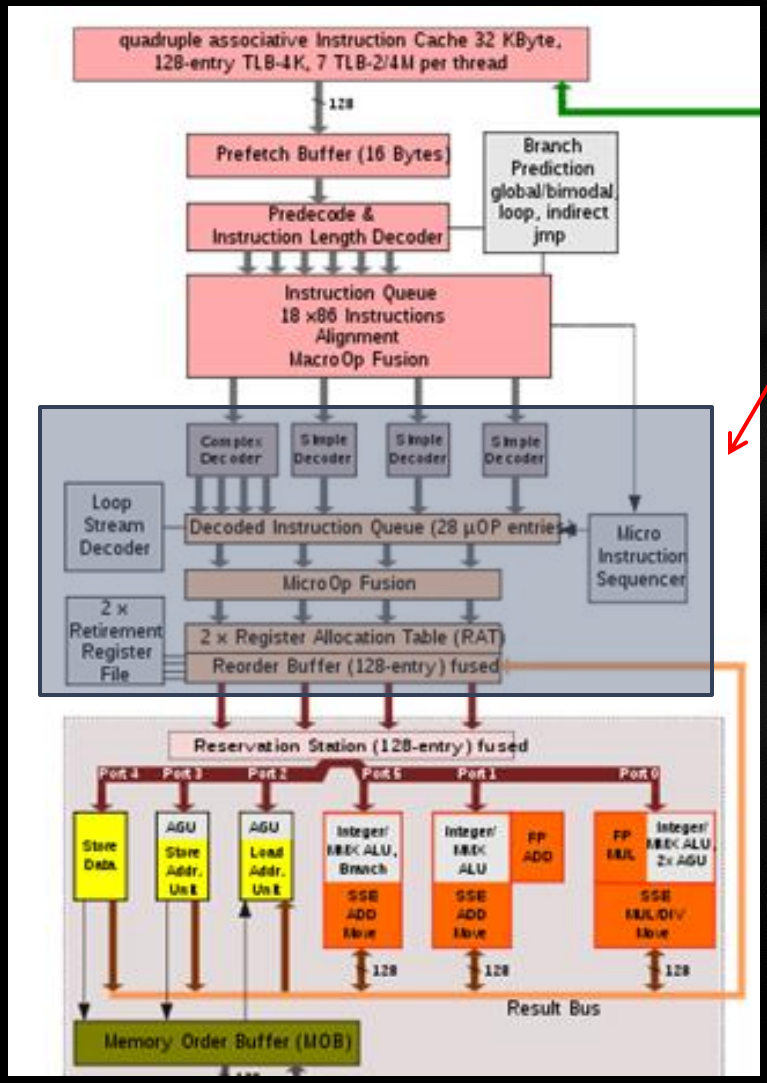
- Fetch
  - Instruction fetched from L2 Cache

High-level Instruction Flow



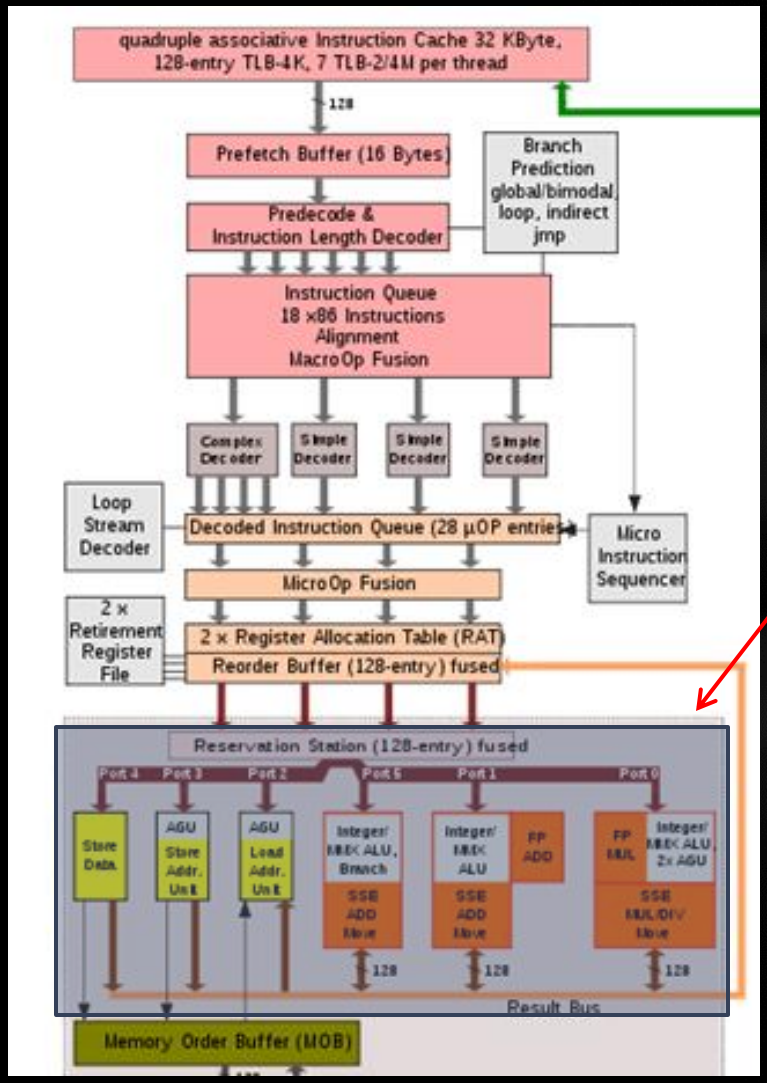
- Fetch
  - Instruction fetched from L2 Cache
- Decode
  - Instructions decoded, pre-fetched and queued
    - 16-byte pre-fetch buffer
    - 18-op instruction que
    - Macro-op fusion occurs
    - Branch Prediction

High-level Instruction Flow



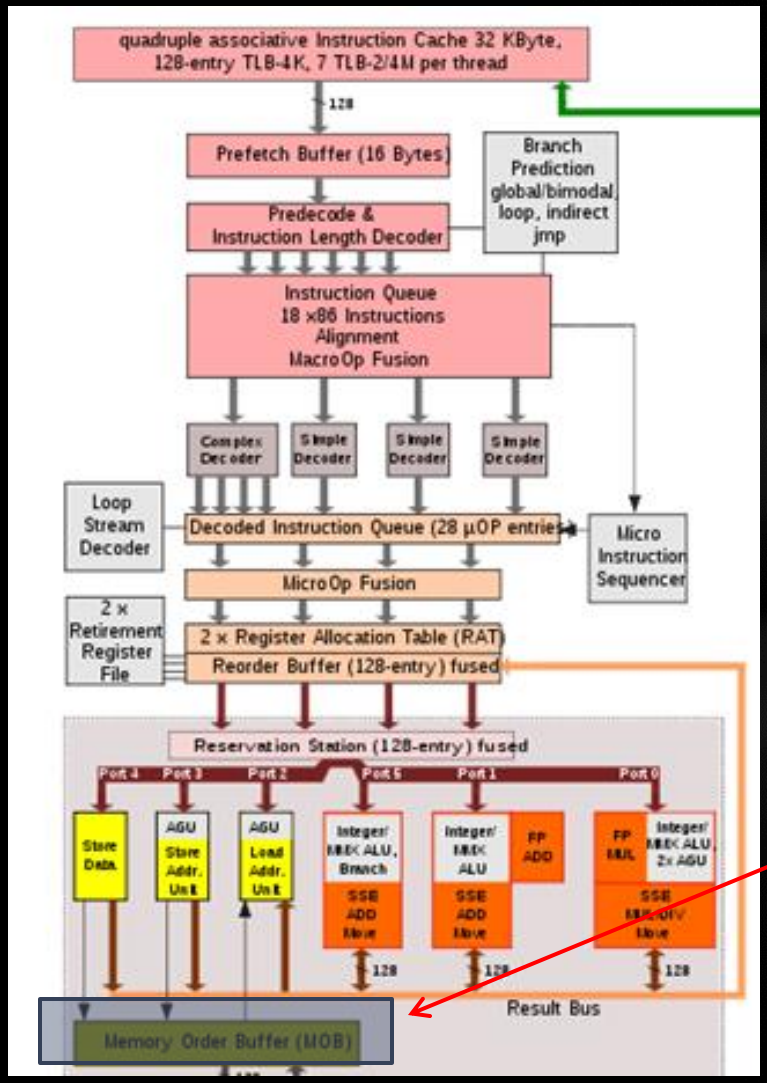
- Optimize
  - Instructions optimized and combined

High-level Instruction Flow



- Optimize
  - Instructions optimized and combined
- Execute
  - Four FPUs
    - MUL, DIV, STOR, LD
  - 3 ALUs

High-level Instruction Flow



- Optimize
  - Instructions optimized and combined
- Execute
  - Four FPUs
    - MUL, DIV, STOR, LD
  - 3 ALUs
- Write
  - MOB ensures in-order writing
  - Results written to private L1/L2 Cache

References

Kanter, David. *Real World Technologies*. 2 Apr. 2008. n.d. http://www.realworldtech.com/page.cfm?ArticleID=RWT040208182719&p=4

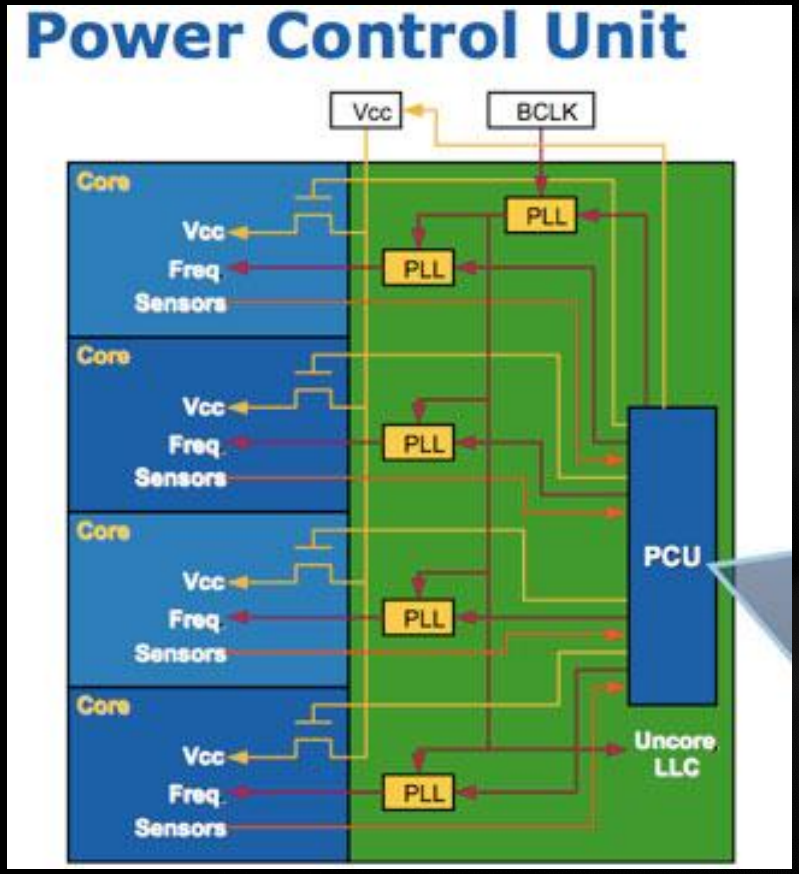
Thomadakis, Michael E. "The Architecture of the Nehalem Processor and Nehalem-EP SMP Platforms." n.d.

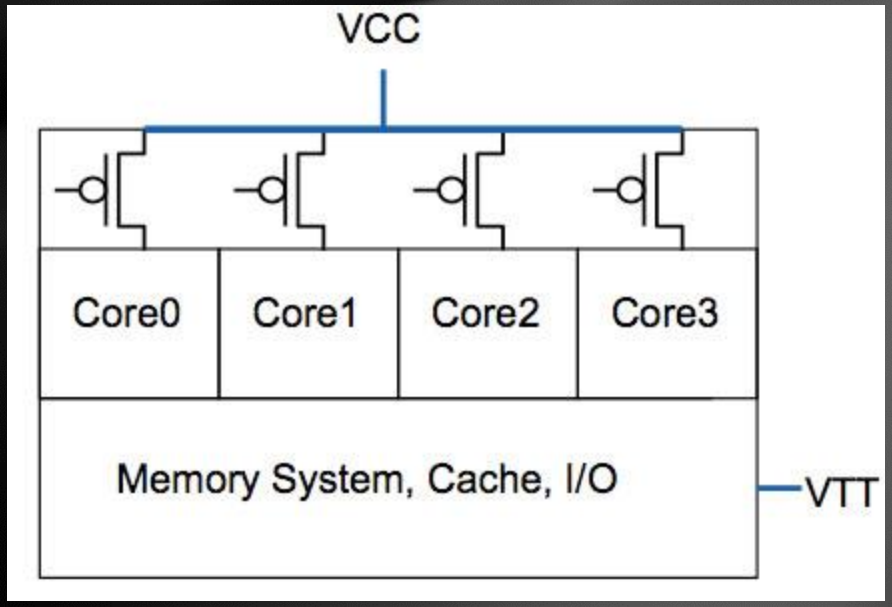
Cepeda, Shannon. Intel Software Network. "Pipeline Speak: Learning More About Intel Microarchitecture"

Nehalem PCU and Turbo Boost Technology

Greg Robinson

How Intel's Power Control Unit Works$_2$





How Nehalem's Turbo Boost Works [2] [3]

- Nehalem's PCU has made Intel's Turbo Boost more effectively utilized
- Past implementations of Turbo Boost haven't been as successful
- Nehalem's Turbo boost is less dependent on the activity of the processor's cores
- Turbo Boost increases a cores frequency by
  - 133MHz (if multiple cores are active)
  - 266MHz(if only a single core is active
- Turbo boost takes advantage of Nehalem's power gates, PLLs and PCU for effective utilization

How Nehalem's Turbo Boost Works 2

Turbo Boost Metrics 1

- Experiment provided by academic article "Evaluation of the Intel Core I7 Turbo Boost feature"
- For the experiment, two test sets were constructed from subsets of the SPEC CPU2006 benchmarks
- Four categories of applications were tested
  - 2 Memory Intensive / Floating Point applications
  - 2 Memory Intensive / Integer applications
  - 2 CPU intensive / Floating Point applications
  - 2 CPU intensive / Integer applications

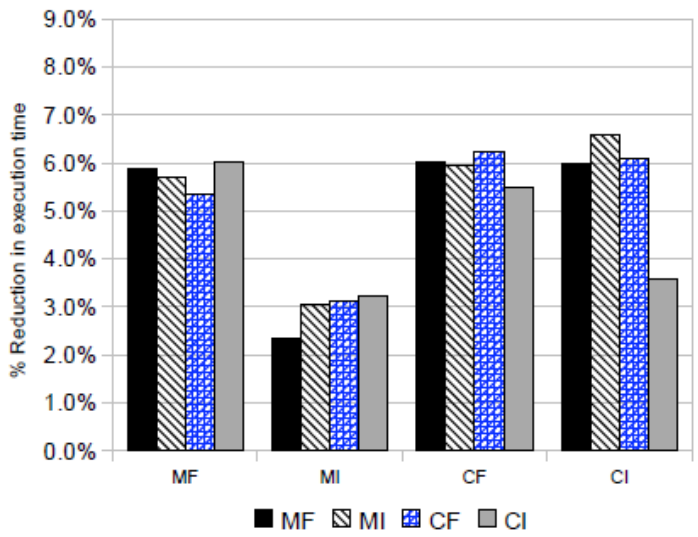
TABLE III
BENCHMARK SETS FOR PAIRED BENCHMARK TESTS

Classification	Set 1	Set 2
MF	Leslie3D	Namd
MI	Omnetpp	Astar
CF	Povray	Bwaves
CI	H264	Hmmer

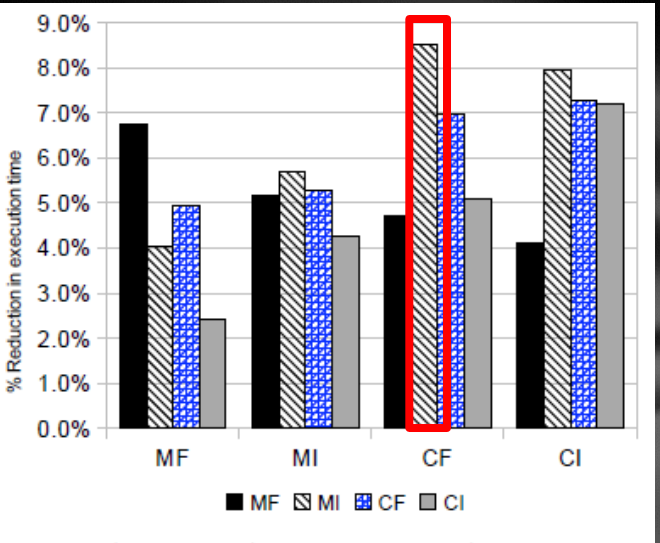
Turbo Boost Metrics 1

- All possible pairs of the four applications were run using one pair per experiment
- The pairs of applications were executed first on the same physical core and then on separate cores
- The pairs of applications were also executed with and without Turbo Boost activated and the speedup was calculated
- For each test, one application in the pair was identified as the principal application and the second was identified as the interfering application

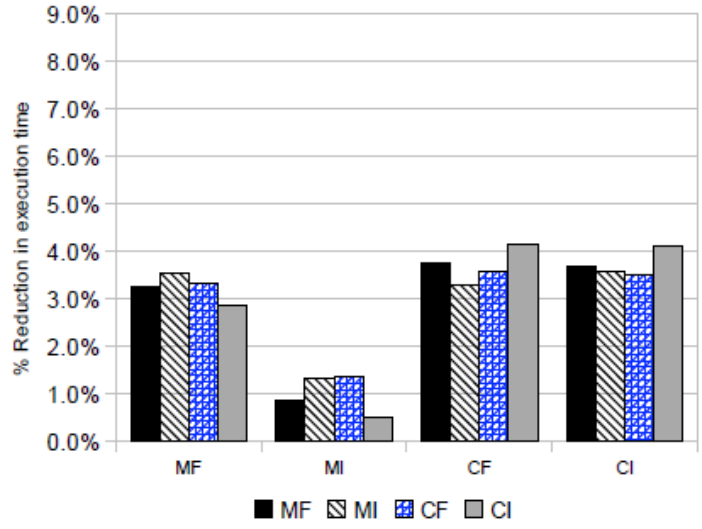
Turbo Boost Metrics 1



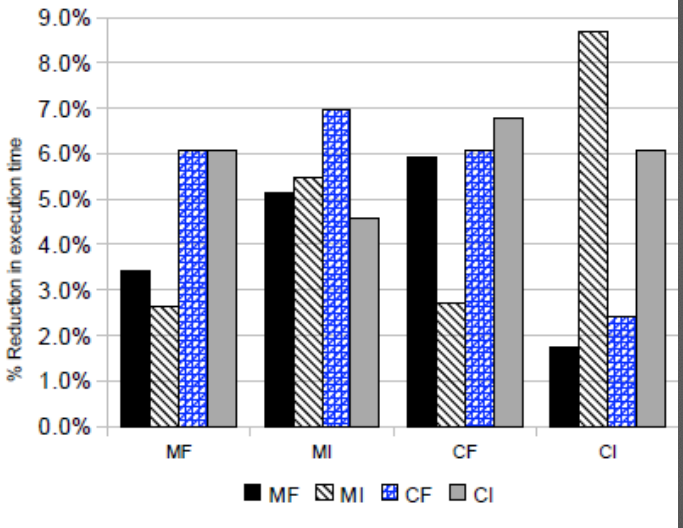
(a) Speedup for Set 1 due to Turbo (Same Core)



(a) Speedup for Set 2 due to Turbo (Same Core)



(b) Speedup for Set 1 due to Turbo (Different Cores)



(b) Speedup for Set 2 due to Turbo (Different Cores)

Turbo Boost Experiment Conclusion 1

- Using the experiment's test results, the conclusion stated that "Turbo Boost can provide on average up to a 6% reduction in execution time."
- The study also found that in all cases Turbo Boost enhanced performance

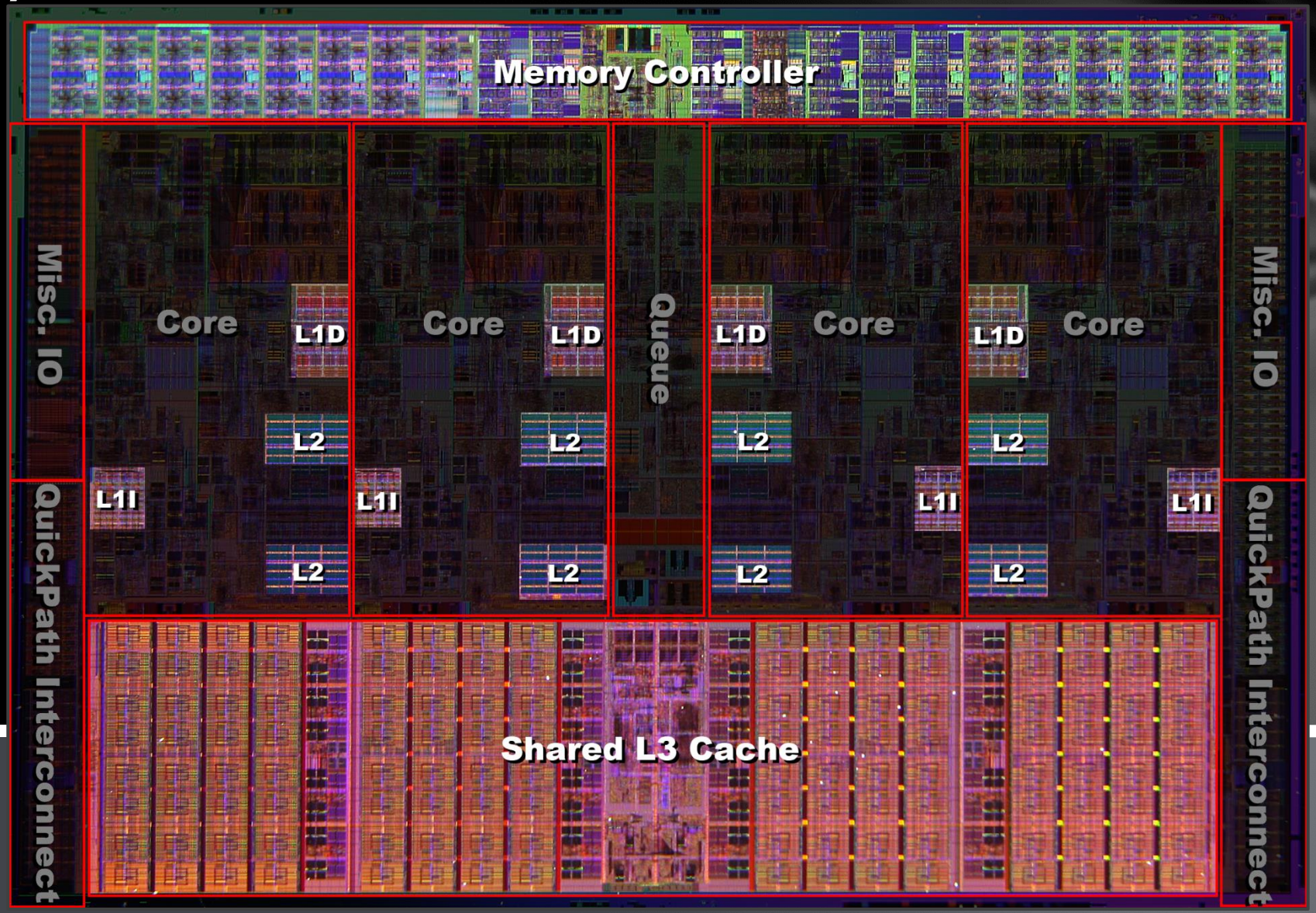
Turbo Boost References

1. Charles, James; Jassi, Preet; Narayan, Ananth; Sadat Abbas and Alexandra Fedorova, "Evaluation of the Intel® CoreTM i7 Turbo Boost feature," *Workload Characterization, 2009. IISWC 2009. IEEE International Symposium on , vol., no., Sept. 2009*
2. Shimpi, Anand L. "Nehalem - Everything You Need to Know about Intel's New Architecture." *AnandTech*. 3 Nov 2009. Web. 5 Mar. 2012. <http://www.anandtech.com/show/2594/12>.
3. Stokes, Jon. "Power Gating and Turbo Mode: Intel Talks Nehalem at IDF." *Ars Technica*. 15 Jan. 2009. Web. 18 Mar 2012. <http://arstechnica.com/hardware/news/2008/08/power-gating-and-turbo-mode-intel-talks-nehalem-at-idf.ars>.

Memory Hierarchy

Matt Burrough

i7 Die [1,2]


Memory Controller
Misc. IO
Misc. IO
QuickPath Interconnect
QuickPath Interconnect
Core
Core
Core
Core
L1D
L1D
L1D
L1D
L2
L2
L2
L2
L1I
L1I
L1I
L1I
L2
L2
L2
L2
Queue
Shared L3 Cache

Memory Controller[3]

- Previous Intel processors used a separate memory controller in the North Bridge, connected via the Front Side Bus
- Nehalem integrates the controller, which allows the cores to access it directly.
- Multi-Processor Nehalem systems are NUMA.

Cache Sizes & Associativity [4,5,6,7]

L1 I:

- 32 KB (per core)
- 4-way set associative

L1 D:

- 32 KB (per core)
- 8-way set associative

L2:

- 256 KB (per core)
- 8-way set associative
- Exclusive

L3:

- 8 MB
- 16-way set associative
- Inclusive

Latencies [4,5]

L1 (D&I): 4 cycles (4)

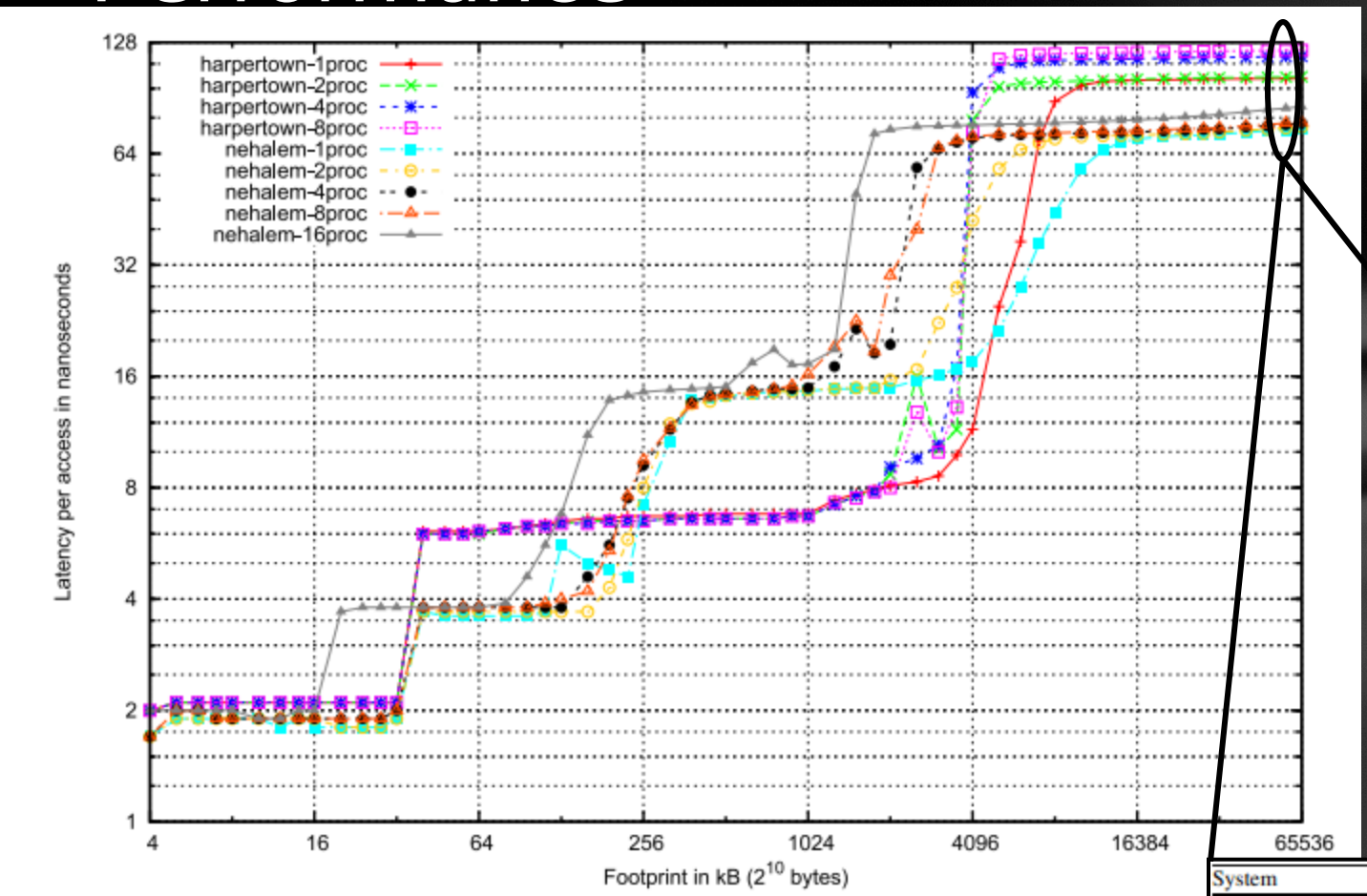
L2: 10 cycles (10)

L3: 35-40 cycles (38)

Comparison [8,9]

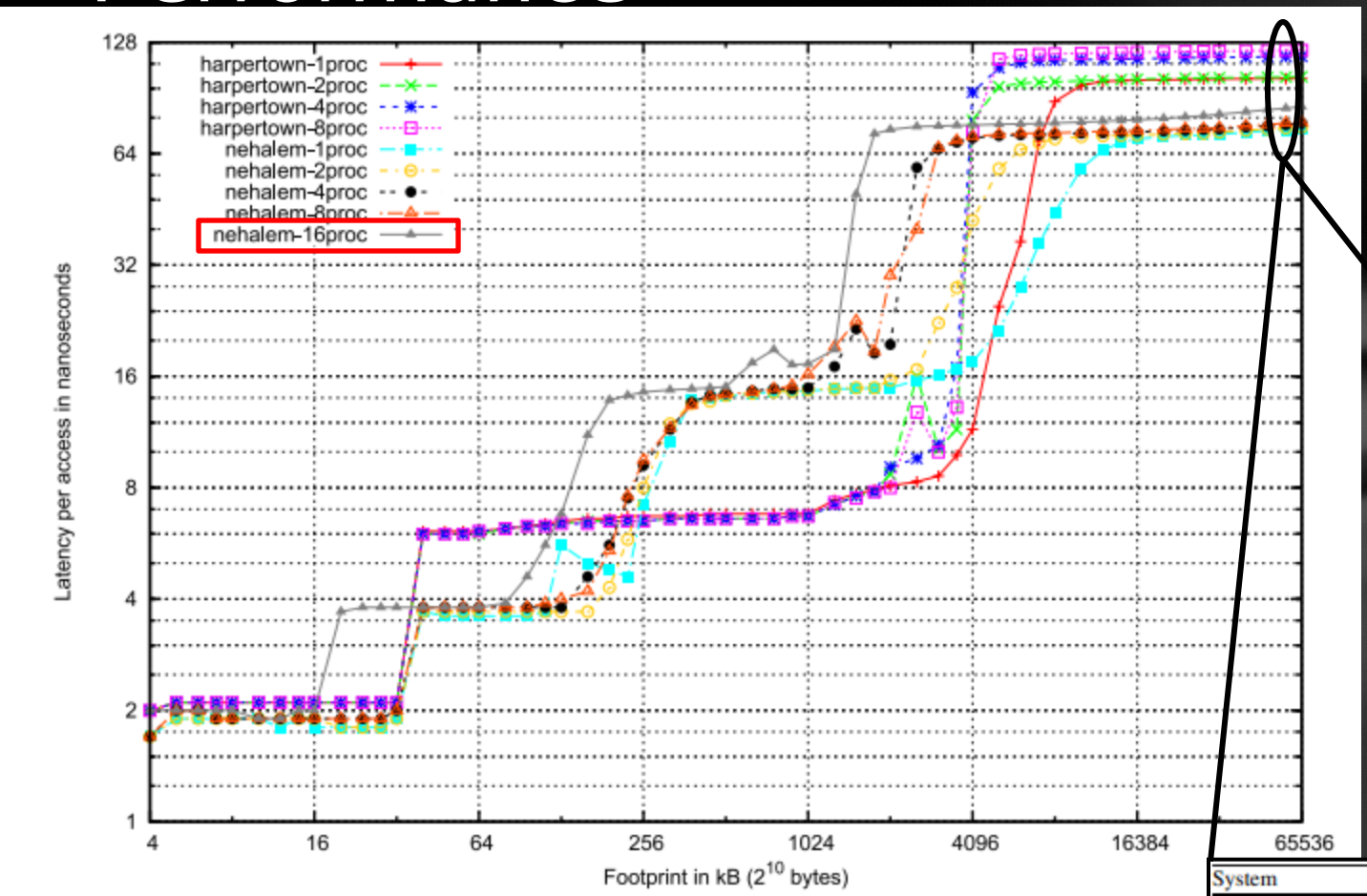
Processor	L1	L2	L3
Conroe (Core 2, 65 nm)	3	14	N/A
Yorkfield (Core 2, 45 nm)	3	15	N/A
Xeon 7400 (Penryn, 45 nm)	3	15	110
AMD Phenom II X6	3	14	55

Performance



System	No of processes	Latency (ns)
Harpertown	1	102
	2	103
	4	117
	8	122
Nehalem	1	74
	2	76
	4	77
	8	78
	16 (SMT)	86

Performance



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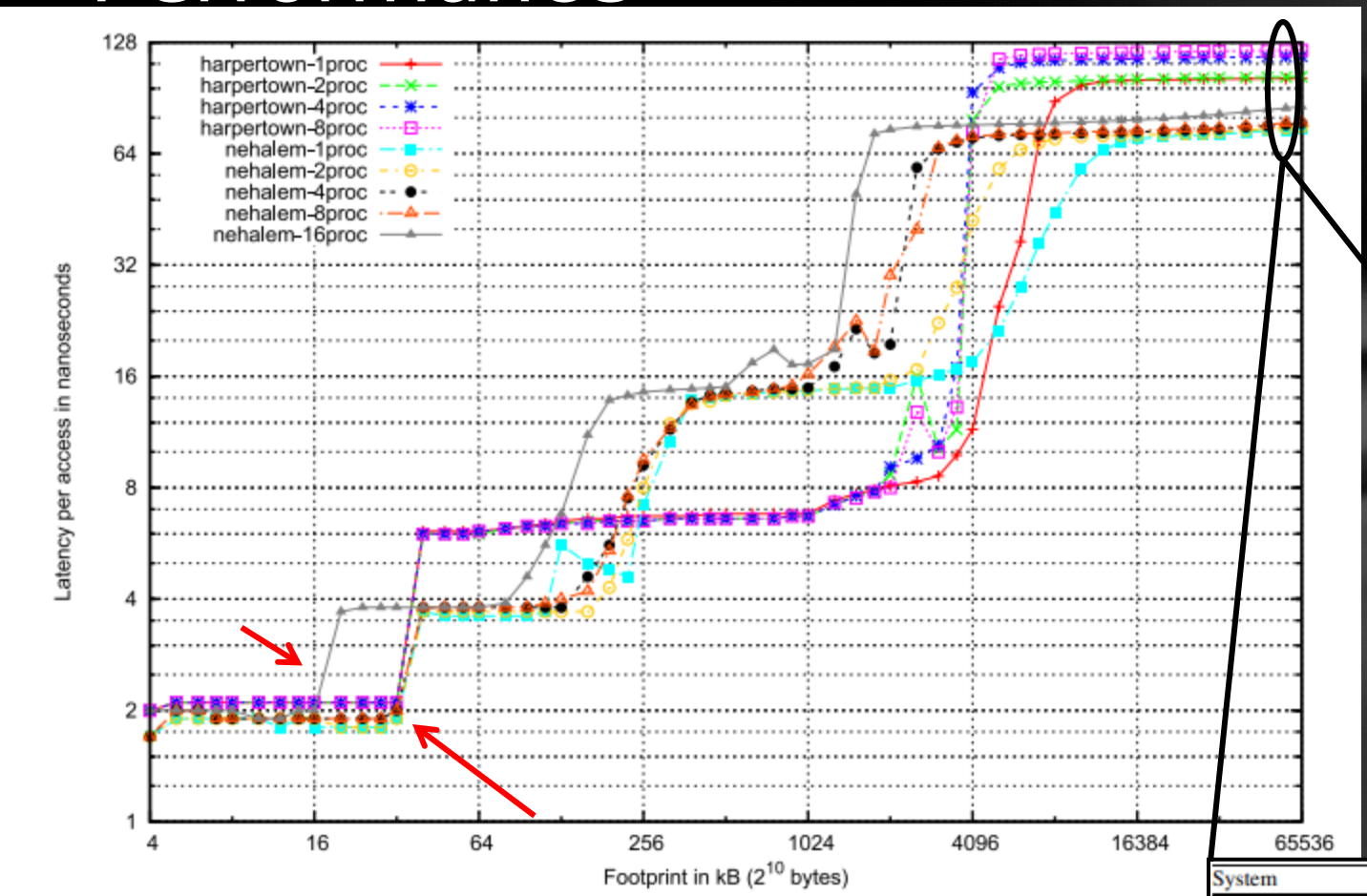

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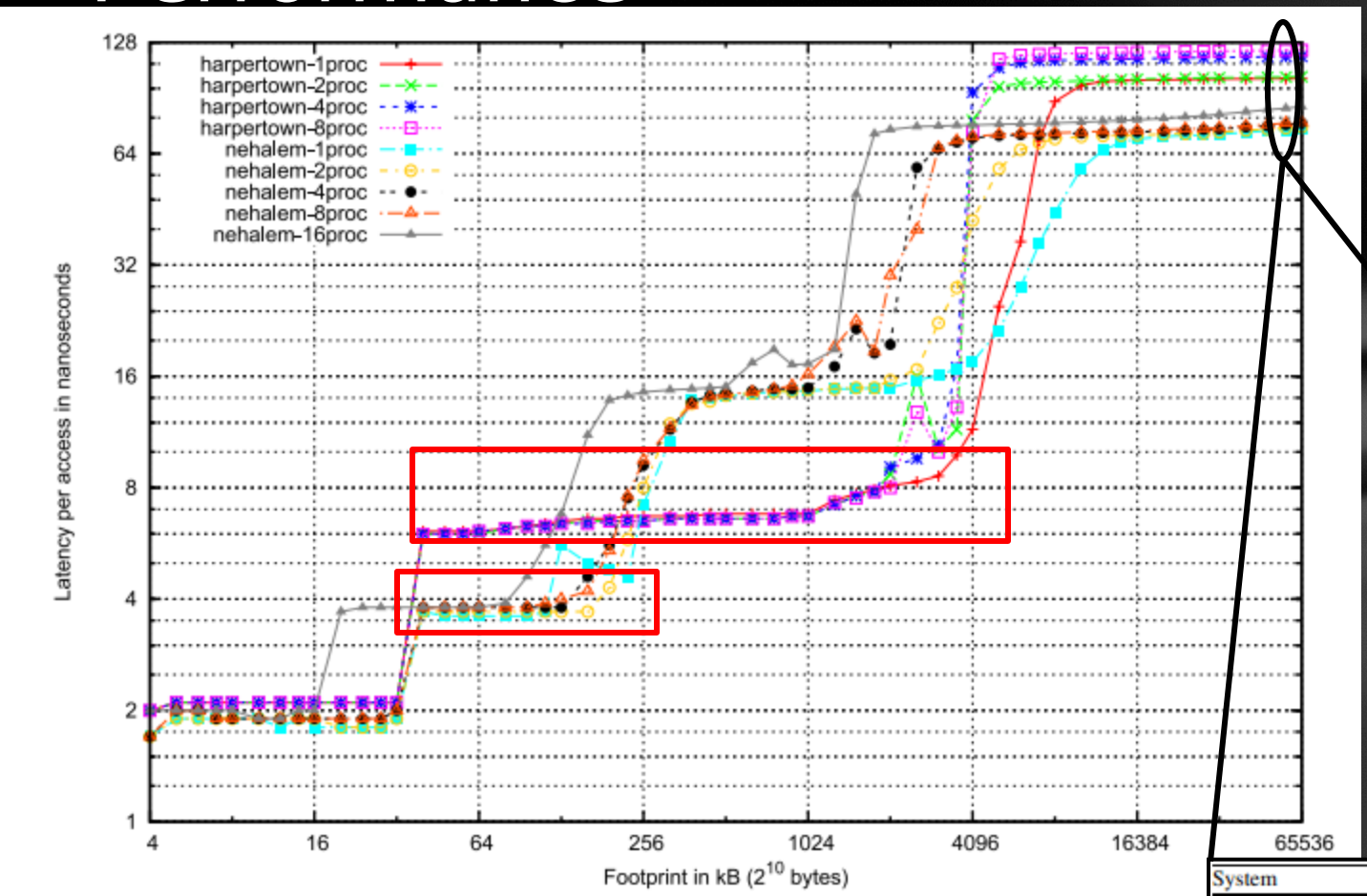

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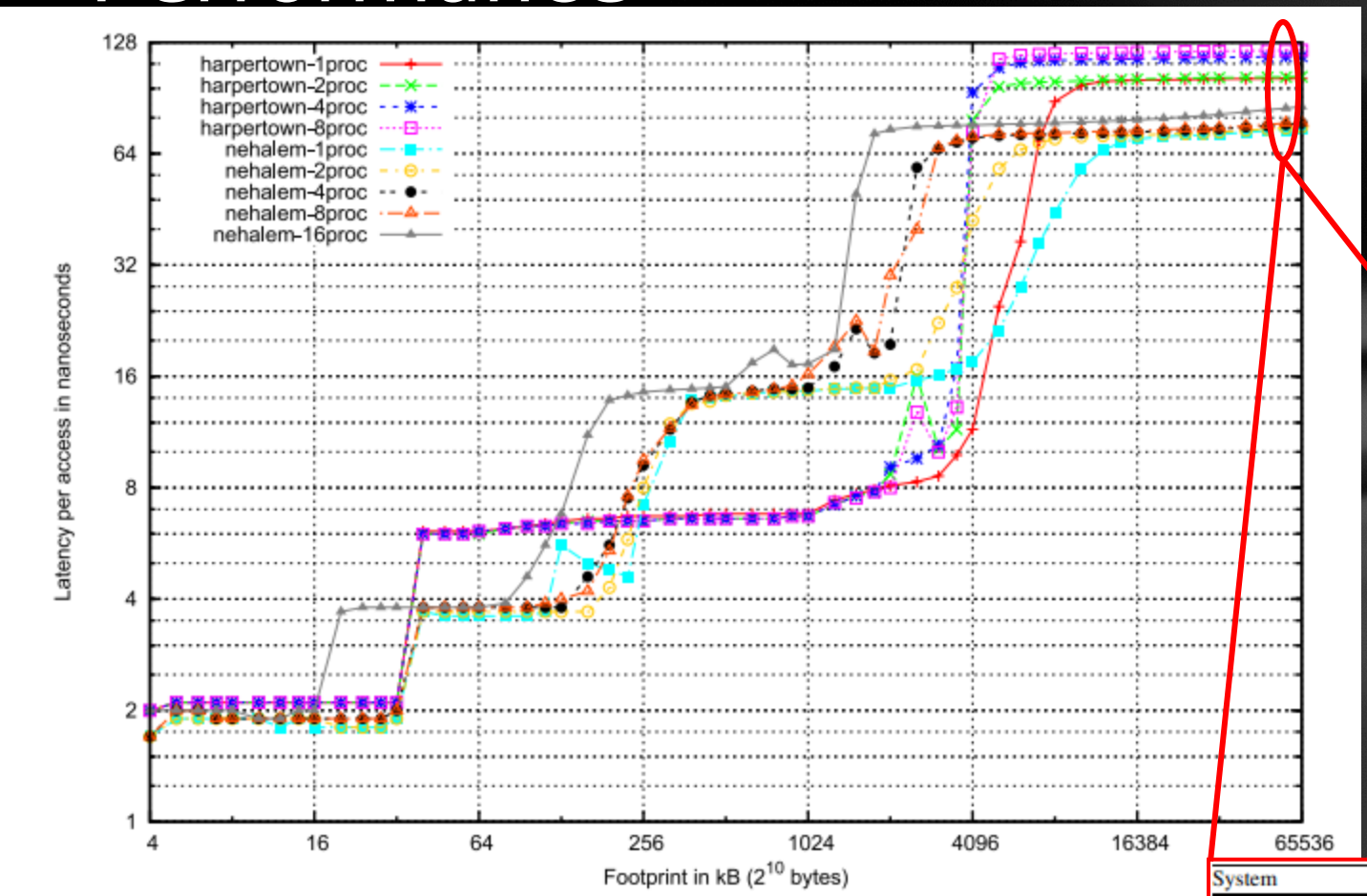

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Memory References

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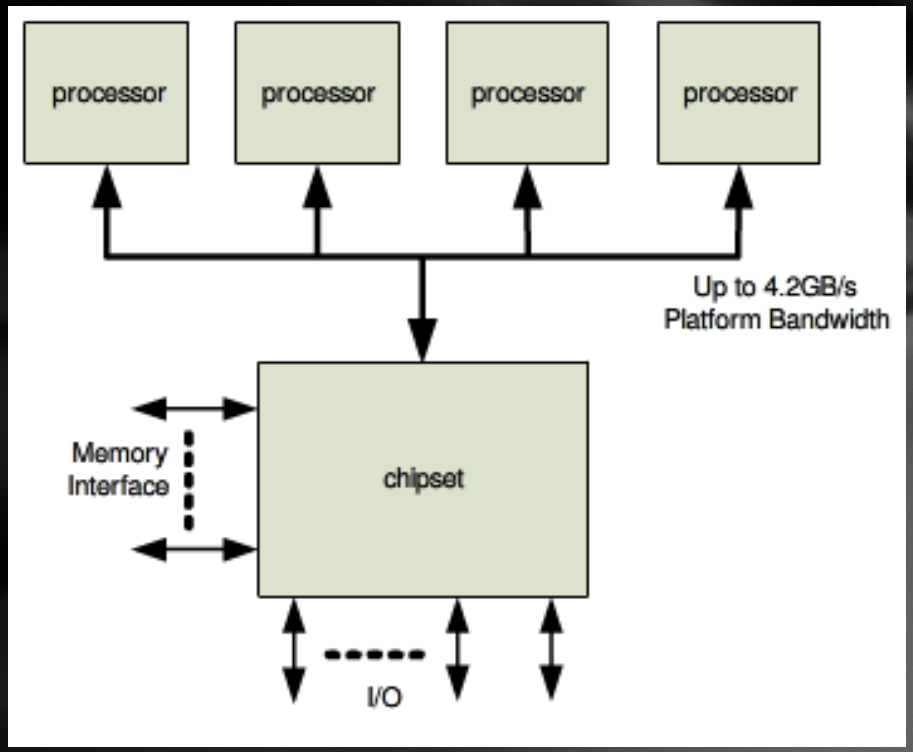
2. Delattre, Franck. "Report: Intel Nehalem Architecture (page 4: Cache Hierarchy)." BeHardware. 28 Oct. 2008. Web. 2 Apr. 2012.
3. Thomadakis, M. “The Architecture of the Nehalem Processor and Nehalem-EP SMP Platforms.” 17 Mar. 2011. Web. 2 Apr. 2012.
4. “Intel® 64 and IA-32 Architectures Optimization Reference Manual.” Intel. June 2011. Web. 24 Mar. 2012.
5. Molka, D., et al. "Memory Performance and Cache Coherency Effects on an Intel Nehalem Multiprocessor System". Parallel Architectures and Compilation Techniques - Conference Proceedings, PACT. 2009. Web. 25 Mar. 2012.
6. Levinthal, David. “Performance Analysis Guide for Intel® Core™ i7 Processor and Intel® Xeon™ 5500 processors.” Intel. 2009. Web. 22 Mar. 2012.
7. Singhal, R. “Inside Intel® Next Generation Nehalem Microarchitecture.” Intel Developer Forum. Intel. 2009. Web. 1 Apr. 2012.
8. Shimpi, Anand L. "The Nehalem Preview: Intel Does It Again." AnandTech. 5 June 2008. Web. 23 Mar. 2012.
9. Shimpi, Anand L. "The Bulldozer Review: AMD FX-8150 Tested." AnandTech. 12 Oct. 2011. Web. 30 Mar. 2012.
10. Bugge, H. O. "An Evaluation of Intel's Core i7 Architecture using a Comparative Approach." Computer Science - Research and Development 23.3-4 (2009): 203-9. Web. 22 Mar. 2012.

QuickPath Interconnect (QPI)

- First developed by Intel in November of 2008.
- Replaces the traditional Front-Side Bus (FSB) interconnect technology.
- Allows bilateral serial communication between CPU cores, memory and other IO devices.

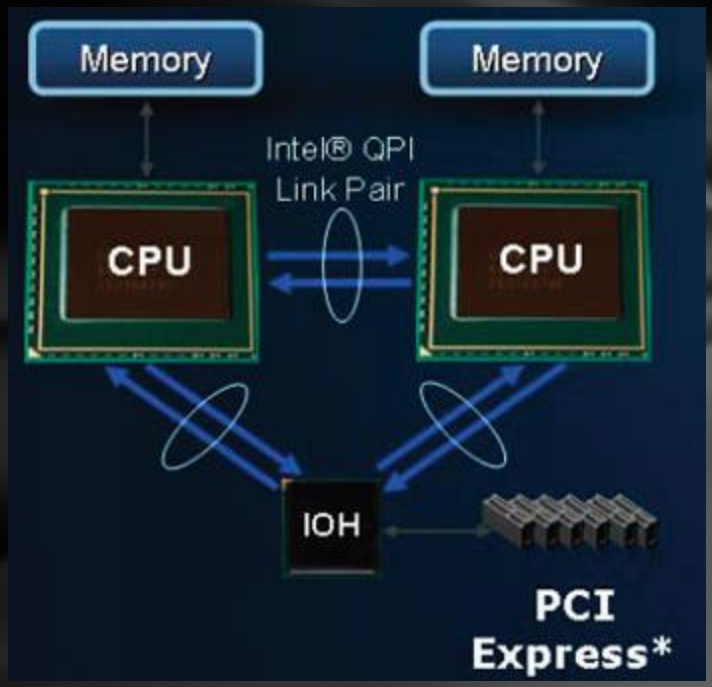
History Front-Side Bus (FSB) interconnect

- One interconnect each device shares.
- Creates a bottleneck when fetching instructions or accessing memory.
- Causes the CPU to waste cycles waiting for information.



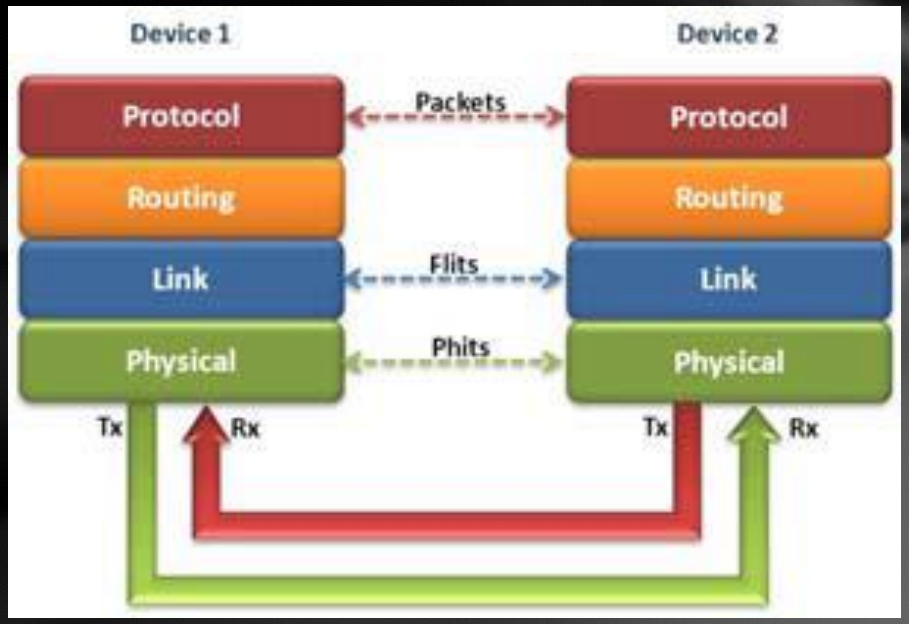
Current Day

- Point to Point Protocol instead of a bus.
- Consists of a single wire pair between each device.
- Able to operate at 2.4 GHz, 2.93 GHz, or 3.2 GHz depending on the operating frequency of the device.



QuickPath Interface

- Physical
- Link
- Routing
- Protocol



Performance

Technology	Speed (GT/s)
Intel Front-side bus	1.6
PCI Express Gen 1	2.5
Fully Buffered DIMM	4
PCI Express Gen 2	5
QuickPath Interconnect	6.4
PCI Express Gen 3	8

References

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- Intel. *Intel*. 2009. Web. 22 Apr. 2012. <http://www.intel.it/content/www/us/en/io/quickpath-technology/quick-path-interconnect-introduction-paper.html>.
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